**Amendments to the Drawings**:

The attached two sheets of drawings include changes to Figs. 1 and 7. These sheets, the first of which includes Figs. 1-3 and the second of which includes Fig. 7, replace the corresponding sheets of the original set. In Fig. 1, we changed "$S_2O_2$" to "$SiO_2$", and in Fig. 7, we have added reference numerals 101 and 103, which were missing from the original drawing.

Attachment: Replacement sheets
Annotated sheets showing changes

## REMARKS/ARGUMENTS

We have amended the claims to address the examiner's objections and to more particularly point out and distinctly claim the invention. After entering the claim amendments presented here, claims 1-6, 8-10, and 17-28 will be pending in this application.

The examiner rejected claims 1-6, 8-10, and 17-28 under 35 U.S.C. §103(a) as being unpatentable over Delwala (U.S. 6,658,173) in view of Johnson et al. (U.S. Publication 2002/0181825) and Nakamura (U.S. 6,448,411).

The examiner admitted that "Delwala does not expressly disclose said optical signal distribution circuit to be designed to provide signals to the microelectronic circuit to be fabricated in the first region of the second semiconductor layer." But we note there is more missing from Delwala than the examiner recognizes. More significantly, Delwala does not even hint at an optical ready substrate, namely, a substrate that includes:

> ... a second semiconductor layer on top of the insulating layer, wherein the second semiconductor layer has a top surface and is laterally divided into two regions including a first region and a second region, the top surface of the first region being of a quality that is sufficient to permit microelectronic circuitry to be formed therein and said second region including an optical signal distribution circuit formed therein, said optical signal distribution circuit made up of semiconductor photonic elements interconnected by an optical waveguide for carrying an optical signal characterized by a wavelength of about 850 nanometers or less, said optical distribution circuit designed to provide signals to the microelectronic circuit to be fabricated in the first region of the second semiconductor layer.

as recited in rejected claim 1.

Stated differently, the claimed invention is a substrate that has two laterally arranged regions, one in which an optical signal distribution network has been fabricated and the other in which microelectronic circuitry is to be fabricated. This language makes clear that the fabrication of the microelectronic circuitry is to take place later and that the optical ready substrate already contains the optical signal distribution circuit in anticipation of the future fabrication of the microelectronic circuitry. We have, however, amended claim 1 to make more explicit that which was implicit in the original wording. In relevant part, amended claim 1 now reads:

> ... the top surface of the first region into which fabrication of microelectronic circuitry has not yet begun and being of a quality that is sufficient to permit microelectronic

> circuitry to be fabricated therein at a later time and said second region including an optical signal distribution circuit formed therein,

The advantages of the claimed optical ready substrate in which the optical signal distribution circuitry has already been fabricated so that it is ready to receive the microelectronic circuitry are explained in the specification:

> One big advantage of separating the optical signal distribution circuitry from the electrical circuitry in this way is that it separates the electrical fabrication processes from the optical fabrication processes. Thus, for example, a company making CMOS circuitry that has optimized its fabrication processes for achieving ultra high precision and very high yields need not be concerned with having to modify its processes and possibly compromise its ultra high precision and high yields to also make optical elements along with the electrical components. Indeed, the company that fabricates the electrical components can simply rely on the expertise of an optical fabrication company to provide the optical elements and to optimize those processes. Developing and optimizing the optical fabrication processes will typically require special expertise and considerable research effort and that may be something that is not within the either the financial or technical ability of the company that fabricates the electrical circuits.
>
> The electrical circuit fabricator can process the optical ready substrate just as though it was a blank substrate, i.e., as a substrate that has no special requirements which must be taken into account when fabricating the electrical components. (Pages 3 and 4)

In contrast, Delwala goes to great lengths to select optical component designs which permit the fabrication of both the microelectronic circuitry and the optical devices at the same time using the same processes. In the Background, Delwala states that:

> It would be desirable to provide active optical waveguide device functionality and/or passive optical waveguide device functionality based largely on the CMOS devices and technology as well as manufacturing methods that allow for simultaneous fabrication of optically active and passive waveguide elements. [emphasis added] (Col. 1, lines 62-67).

The device designs that Delwala has selected enabled him to achieve this desired objective. This was made clear at various places in the Delwala specification including the following:

> The same CMOS-based manufacturing process, described herein, can be used to fabricate the active optical waveguide devices 150, the electronic devices 5101, and the passive optical waveguide devices 800 within the integrated optical/electronic circuit 103 often using the same processing steps as described herein. As such, the devices that can perform the pure optical functions 10, the pure electronic functions 12, and the opto-electronics functions 14 can be produced concurrently, on the same wafer 152, and using the same manufacturing process.
>
> The passive optical waveguide devices 800, the electronic devices 5101, and the active optical waveguide devices 150 can each be fabricated using standard CMOS processing techniques and technology. In one embodiment, the passive optical waveguide devices 800, the electronic devices 5101, and the active optical waveguide

> devices 150 are described as being fabricated on a single Silicon-on-Insulator (SOI) wafer 152. For example, pure electronic devices such as field effect transistors (FETs) can be deposited and/or etched on the SOI wafer 152. The passive optical waveguide devices 800 and the active optical waveguide devices 150 can be simultaneously deposited and/or etched on the SOI wafer 152. The masks, and the positioning equipment, that are used for etching active optical waveguide devices 5101 can also be used to etch the passive optical waveguide devices 800 and the active optical waveguide devices 150 as described herein. [emphasis added] (Col. 10, line 62 to col. 11, line 20).

And again, towards the end of the specification Delwala notes that:

> Electronic devices 5101, active optical waveguide devices 150, and passive optical waveguide devices 800 can each be fabricated with FET, HEMT, and other known semiconductor optical waveguide devices 100 using CMOS, SOI, and VLSI technologies. VLSI and CMOS masks are used to simultaneously deposit and/or etch on a single SOI wafer 152 one or more passive optical waveguide devices 800, one or more active optical waveguide devices 150, and/or one or more electronic devices 5101. [emphasis added] (Col. 44, lines 11-19).

The other references on which the examiner relies, namely, the Johnson application and the Nakamura patent, do not supply that which is missing from Delwala. Indeed, in the case of the Johnson application, to the extent that Johnson teaches anything about the order in which optical components and microelectronic components are formed in a substrate, that order is the reverse of that which is recited by claim 1. This is because Johnson forms his optical components using materials (e.g. III-V semiconductor compounds) that would be damaged by the high temperatures required by typical microelectronic fabrications processes. This is explicitly pointed out in the following passages form Johnson:

> [0001] ...Optical devices are typically not formed on silicon substrates. Instead, optical circuits are typically formed on compound semiconductors such as GaAs or Indium Phosphide.
>
> [0167] Once hybrid structure 4200 has been formed, electronic circuitry can be created by forming electronic components 4256 and 4268 in substrate 4201 and island 4204, respectively. Alternatively, component 4256 may be formed in substrate 4201 prior to the formation of island 4204. Either way, the components can be interconnected by appropriate metallization 4270 as shown in FIG. 46, resulting in hybrid integrated circuit device 4215.
>
> [0168] Component processing in materials such as monocrystalline silicon is typically carried out at temperatures above about 800° C., while component processing in compound semiconductor materials such as GaAs is typically carried out at lower temperatures, between about 300° C. and about 800° C., and components formed in GaAs would be damaged by the higher temperatures of silicon processing (although the unprocessed GaAs itself would not be damaged). Therefore, preferably components such

> as component 4256 are formed first in silicon substrate 4201 using high-temperature processing. Components such as component 4268 are then formed in the GaAs island 4204 at the lower processing temperatures, which will not damage the already formed silicon components 4256. [emphasis added] (Page 17).

Thus, Johnson actually teaches away from the claimed invention.

For the reasons stated above, we believe that the claims are allowable and therefore ask the Examiner to allow them to issue.

Our records indicate that the copies of Form PTO-1449 which were previously submitted on November 3, 2003 have not been initialed and returned to us. For your convenience we have also enclosed a copy of the previously submitted PTO-1449 and ask you to also initial and return that form as well.

Please apply any charges not covered, or any credits, to Deposit Account No. 08-0219.

Respectfully submitted,

Date: July 25, 2005

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App No.: 10/623666
Docket No.: 0107262.00202US1
Inventor: Claes BJORKMAN et al.
Title: OPTICAL READY SUBSTRATES
ANNOTATED SHEET





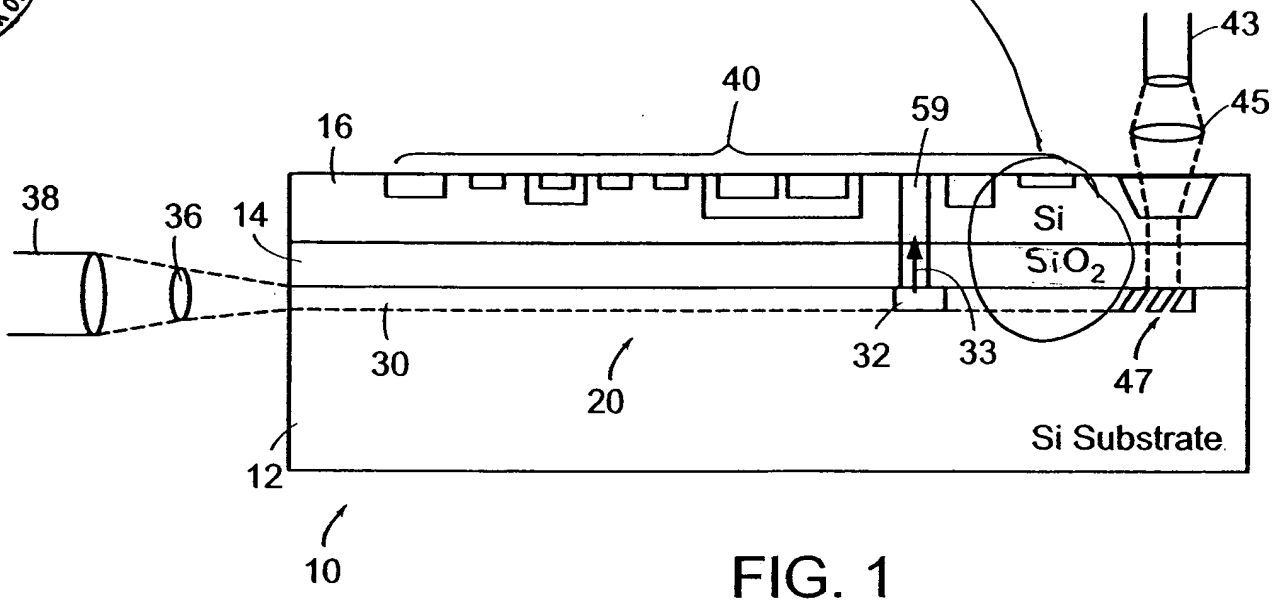


FIG. 1

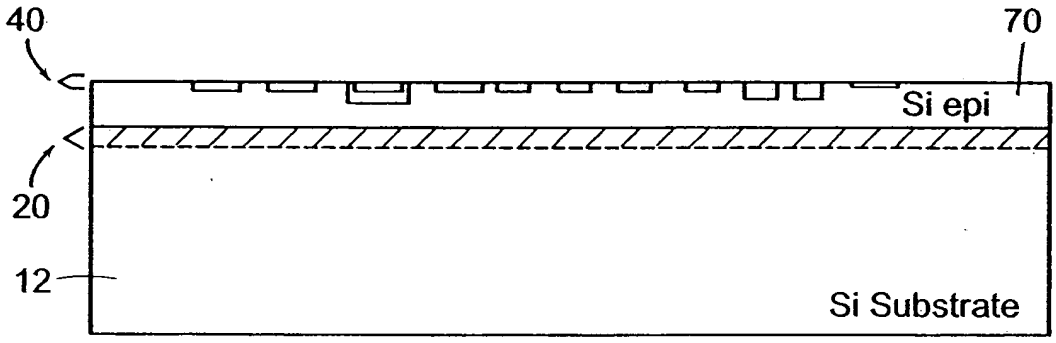


FIG. 2

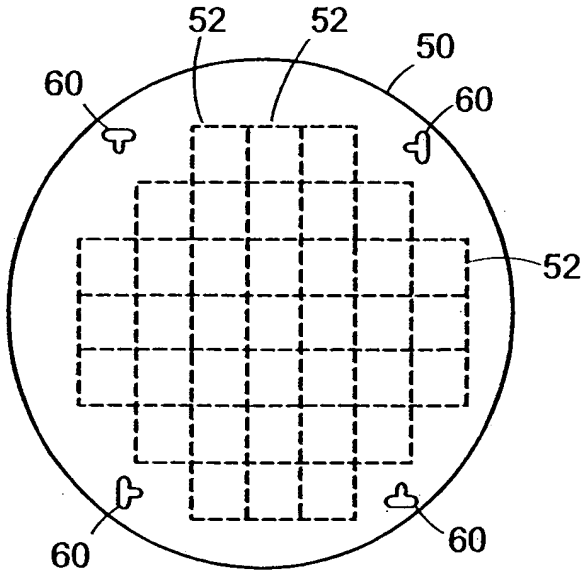


FIG. 3

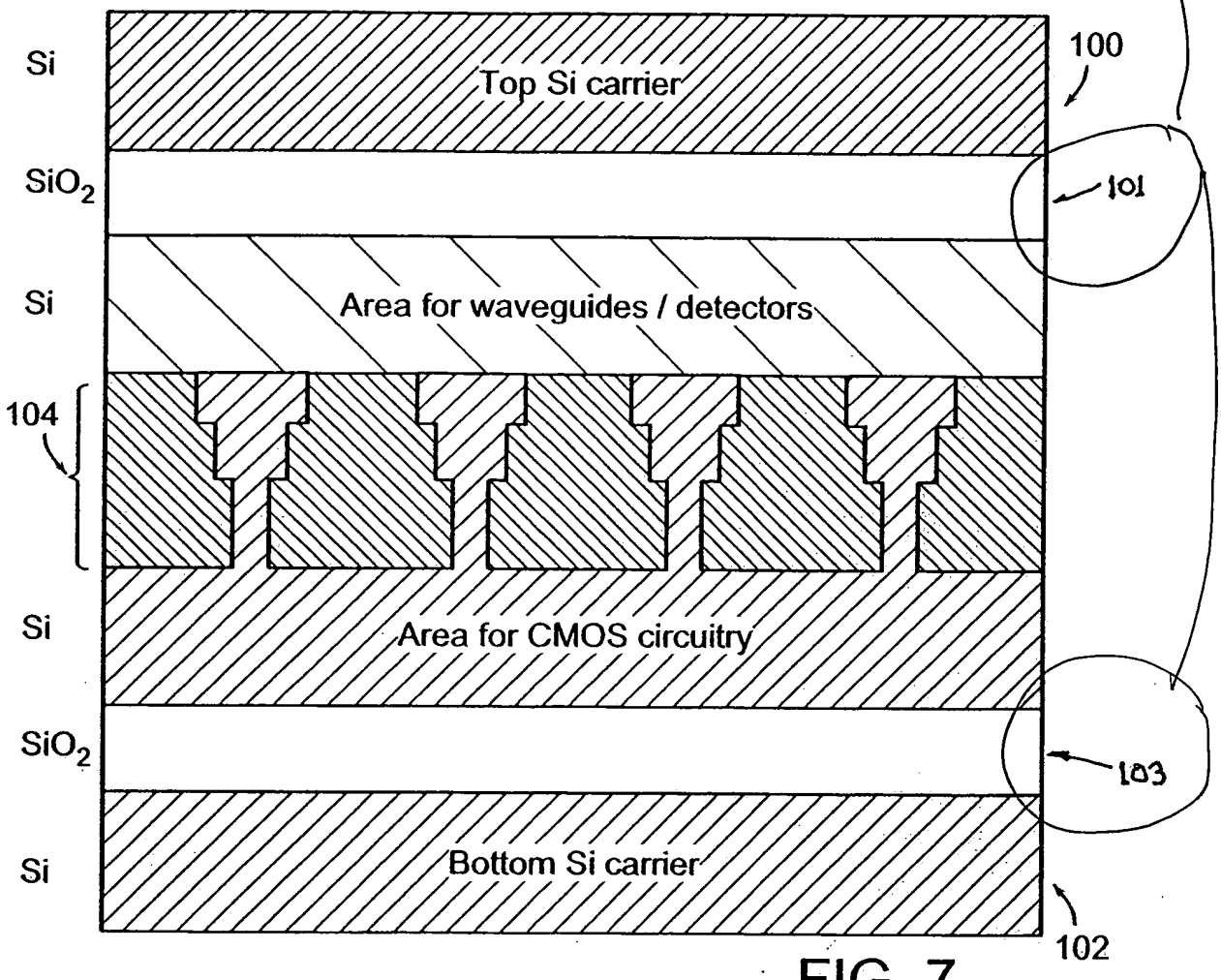
Si
Top Si carrier
100
$SiO_2$
101
Si
Area for waveguides / detectors
104
Si
Area for CMOS circuitry
$SiO_2$
103
Si
Bottom Si carrier
102

FIG. 7